D K Bhargav Achary

Computer Architecture & Performance Engineer

Pune, India | Open to Pune District roles

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Professional Summary

- Performance engineer across IBM Power, AMD Ryzen, and Qualcomm Hexagon DSP, specializing in C/C++ performance modeling, workload characterization, PMU/PMC analysis, and simulator-to-RTL correlation.
- MS in Computer Science & Engineering with ACM-published hardware-PMC research and experience in pre-silicon modeling, performance validation, and processor, cache, memory and interconnect analysis.

Technical Expertise

Architecture:	Microarchitecture, Cache / Memory Hierarchy, Cache Coherence, Interconnects, Virtual Memory; x86, Arm, VLIW/DSP
Performance:	Performance Modeling, Workload Characterization, PMU / PMC Analysis, Simulator-to-RTL Correlation, Bottleneck Analysis, Bandwidth / Latency Analysis
Software / Tools:	C/C++, Python, Assembly, Bash; SystemVerilog, RTL Debug; Linux, gem5, perf, Verdi, Git
AI / Workloads:	DNN Workload Analysis, PyTorch, scikit-learn, Statistical Analysis, Plotly

Industry Experience

IBM India Private Limited
Bengaluru, Karnataka, India

Chip Designer / Hardware Developer | Power Systems Performance *Oct 2024 - Oct 2026*

- Developed a modular C/C++ Snoop Filter in a gem5-derived simulator with timing hooks and minimal rebase overhead.
- Debugged LSU/IU simulator uops and closed timing and functional gaps, improving RTL correlation from 93% to 95%.
- Built a simulation-execution comparison tool using LLM-assisted workflows to identify, map, and debug microarchitectural execution divergences.
- Analyzed IBM Power fabric bandwidth/latency and validated PMU behavior for accurate system-level profiling.

AMD India Private Limited
Bengaluru, Karnataka, India

Senior Silicon Design Engineer - Ryzen Core Performance Modeling Team *Dec 2023 - Jun 2024*

- Supported Ryzen CPU core performance-modeling infrastructure, including flow automation and PMC data post-processing.
- Executed regressions and studies on microarchitectural changes, debugging simulator-to-RTL correlation issues and non-correlating PMC counters.

Qualcomm India Private Limited
Bengaluru, Karnataka, India

Hardware Engineer - Hexagon DSP Performance Team *Nov 2021 - Dec 2023*

- Independently drove pre-silicon performance verification for 3+ Hexagon DSP cores against design specifications, delivering comprehensive results ahead of schedule.
- Characterized DSP workloads using statistical analysis and Plotly visualizations to expose performance bottlenecks.
- Developed directed cache-feature tests to validate system-level performance against design specifications.

Education

MS, Computer Science & Engineering	Indian Institute of Technology Hyderabad	2018 - 2021	Hyderabad, India
BTech, Electronics & Comm. Engineering	Biju Patnaik University of Technology	2010 - 2013	Odisha, India

Earlier Technical & Research Experience

Indian Institute of Technology Hyderabad *Hyderabad, Telangana, India*
Graduate Researcher *Dec 2018 - Jun 2021*
- Published ACM research on a hardware-PMC side-channel attack that profiled cache, branch, and instruction events and used machine learning to infer DNN layer types with over 90% accuracy.

DRDO (Ministry of Defence) *Hyderabad, Telangana, India*
Senior Technical Assistant-B *Jul 2016 - Jan 2018*
- Provided technical and computational support for experimental design and execution in coordination with HPC and resource teams.
- Managed workstation system administration and supported deployment of an OpenStack private cloud.

Indian Institute of Technology Guwahati *Guwahati, Assam, India*
Junior Research Fellow *Jul 2015 - May 2016*
- Selected for an MHRD-funded research position in a doctoral program and served as a Teaching Assistant for two undergraduate CSE courses.

Achievements

2026 Won the IBM India Systems Development Lab-wide **Bob-a-thon** as a **solo developer**, delivering a working agentic-coding prototype from concept in one day and outperforming **100+ multi-member teams**.

Projects

DNN Layer Profiling via Hardware Performance Counters *Aug 2019 - Jun 2021*
Research Advisor: Dr. Biswabandan Panda, then IIT Kanpur; now IIT Bombay *IIT Hyderabad*
- Characterized DNN hardware-PMC traces using statistical analysis and Python plots to identify layer signatures.
- Designed a PMC-based side-channel attack to reverse-engineer DNN layer distributions.
- Executed the attack with over 90% layer-identification accuracy without prior knowledge of the model architecture, leading to an ACM AIMLSystems ’21 publication.

CardNiti.com *Early 2026 - Present*
Independent Project *cardniti.com*
- Identified gaps in existing credit-card comparison tools and architected CardNiti as an end-to-end comparison and wallet-planning platform spanning discovery, normalized card data, decision logic, and web presentation.
- Normalized credit-card terms across 172 cards from 25 banks and designed CardMatch to recommend personalized 3-card wallet portfolios using transparent weighted multi-criteria scoring.
- Built and shipped CardNiti using Codex, Claude, and Antigravity in an agentic development workflow, rapidly learning and applying the required web, data, testing, and validation technologies.

Selected Publication

[1] D. K. B. Achary, R. S. C. Teja, S. Mittal, B. Panda, and C. K. Mohan, “Inferring DNN layer-types through a hardware performance counters based side channel attack,” in *Proc. 1st ACM International Conference on AI-ML Systems (AIMLSystems ’21), Bengaluru, India, Oct. 2021, pp. 4:1–4:7*.
[Paper] doi: 10.1145/3486001.3486224 [Presentation]